

## Single-Thread Processor

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40						
PC	A	B	C	D	E	E	E	E	E	F	F	F	F	F	F	F	F	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G									
FETCH	A	B	C	D	D	D	D	D	D	E	E	E	E	E	E	E	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F									
DECODE	A	B	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E									
OPERAND	A	B	B	B	B	B	B	B	B	C	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D									
EXECUTE																																														
ADDRESS																																														
MEM																																														
MEM																																														
MEM																																														
WRITEBACK																																														
memory in use																																														

Figure 1a

## Single-Thread Processor with Data Cache

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40						
PC	A	B	C	D	E	E	F	F	G	G	H	H	I	I	I	J	J	K	K	K	L	L	M	M	M	M	M	M	N	N	N	O	O	P	P	O	O									
FETCH	A	B	C	D	D	D	D	D	E	E	F	F	G	G	G	H	H	I	I	J	J	K	K	L	L	M	M	M	M	N	N	N	O	O	O	O	O	O								
DECODE	A	B	C	C	C	D	D	D	E	E	F	F	G	G	G	H	H	I	I	J	J	K	K	L	L	M	M	M	M	N	N	N	M	M	M	M	M	M								
OPERAND	A	B	B	B	B	C	C	C	D	D	E	E	F	F	F	G	G	G	H	H	I	I	J	J	K	K	L	L	M	M	M	N	N	N	M	M	M	M	M							
EXECUTE	A	B	B	B	B	C	C	C	D	D	E	E	F	F	F	G	G	G	H	H	I	I	J	J	K	K	L	L	M	M	M	N	N	N	M	M	M	M	M							
ADDRESS																																														
WRITEBACK																																														

Figure 1b

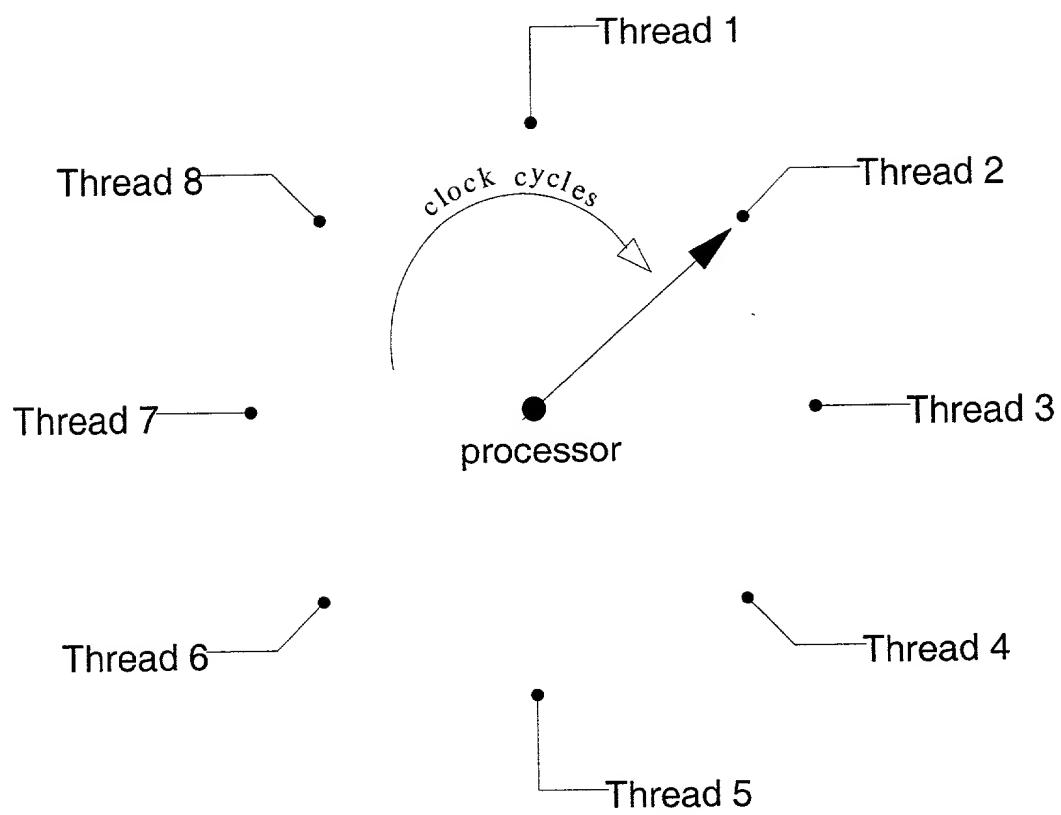


Figure 2

## Four-Thread Processor

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4		
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4C	1D	2D	3D	4D	1E	2D	3D	4D	1E	2E	3E	4E		
FETCH	1A	2A	3A	4A	1B	2B	2B	3B	3B	3B	4B	1C	1C	2C	2C	3C	3C	4C	4C	4C	4C	1D	1D	2D	2D	3D	4D	1E		
DECODE	1A	2A	3A	4A	1B	1B	1B	2B	2B	3B	3B	4B	4B	1C	1C	1C	2C	2C	3C	3C	4C	4C	1D	1D	2D	2D	3D	4D		
OPERAND	1A	2A	3A	4A	4A	4A	1B	1B	2B	2B	3B	3B	4B	4B	1C	1C	1C	2C	2C	3C	3C	4C	4C	1D	1D	2D	2D	3D		
EXECUTE	1A	2A	3A	3A	3A	4A	4A	4A	1B	1B	2B	2B	3B	3B	4B	4B	1C	1C	1C	2C	2C	3C	3C	4C	4C	1D	1D	2D		
ADDRESS	1A	2A	2A	3A	3A	4A	4A	4A	1B	1B	2B	2B	3B	3B	4B	4B	1C	1C	1C	2C	2C	3C	3C	4C	4C	1D	1D	2D		
MEM	1A	1A	2A	2A	3A	3A	3A	3A	1B	1C																				
MEM																														
WRITEBACK																														
memory in use	1	1	1	1	2	2	2	3	3	3	4	4	4	1	1	1	2	2	3	3	3	4	4	1	1	2	2	3	3	

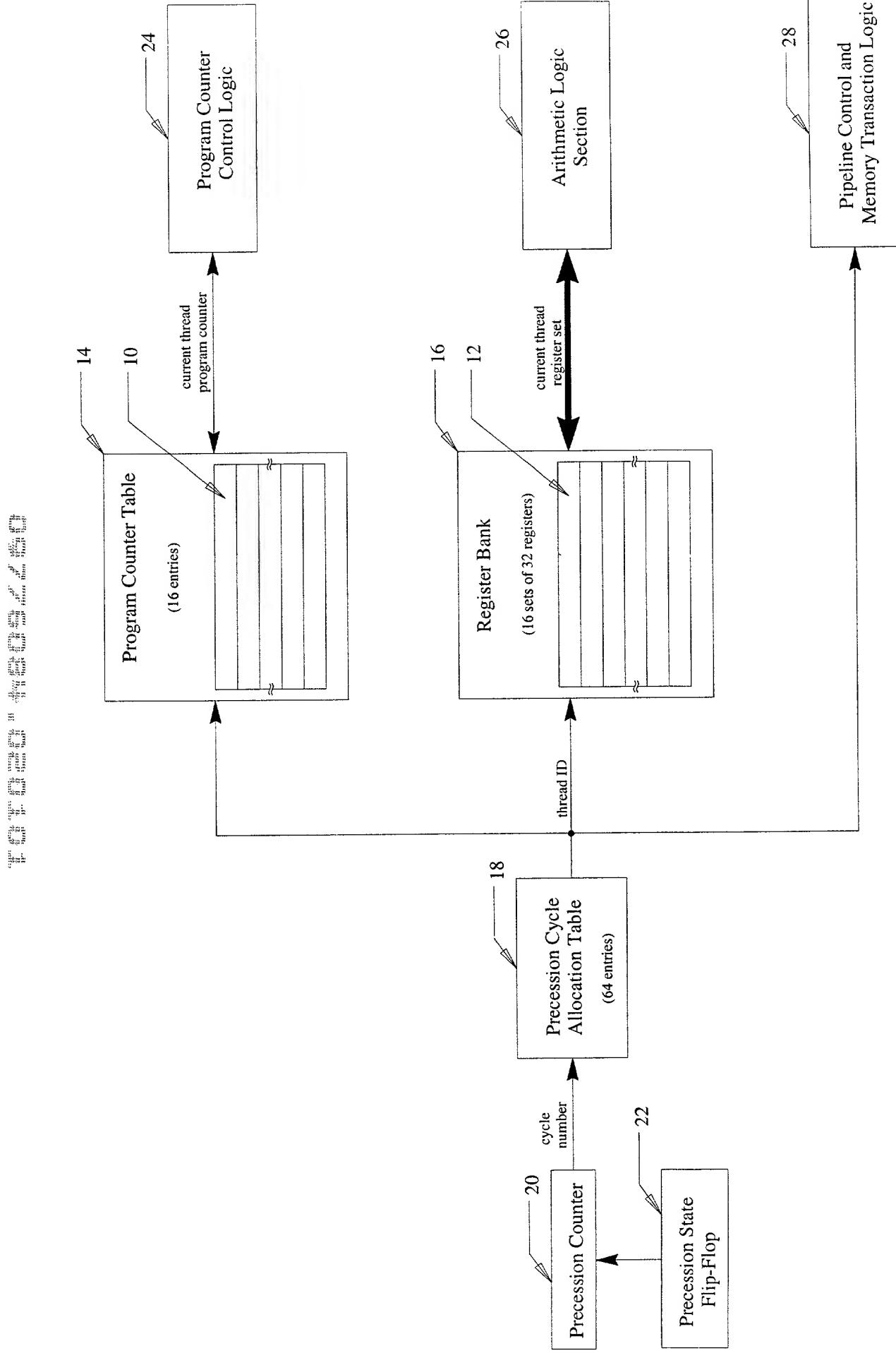
Figure 3a

## Four-Thread Processor with Banked Memory

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1D	2D	3D	4D	1E	2D	3D	4D	1E	2E	3E	4E
FETCH	1A	2A	3A	4A	1B	1B	2B	3B	3B	3B	4B	1C	1C	2C	3C	4C	1D	1D	2D	3D	3D	4D	4D	1E	1E	2E	3E	
DECODE	1A	2A	3A	4A	1B	2B	2B	3B	4B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E	1F	2F	3F	4F		
OPERAND	1A	2A	3A	4A	1B	1B	1B	2B	3B	3B	4B	1C	1C	2C	3C	4C	1D	1D	2D	3D	4D	1E	1E	2E	3E	4F		
EXECUTE	1A	2A	3A	4A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E	1F	2F	3F	4F			
ADDRESS	1A	2A	3A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E	1F	2F	3F	4F			
MEM	1A	1A	2A	3A	4A	1B	1B	2B	3B	4B	1C	1C	2C	3C	4C	1D	1D	2D	3D	4D	1E	1E	2E	3E	4E	1F	2F	
MEM																												
WRITEBACK																												
memory1 in use	1	1	1	3	3	3	1	1	3	3	1	1	3	3	1	1	3	3	1	1	3	3	1	1	1	3		
memory2 in use	2	2	2	4	4	4	2	2	4	4	2	2	4	4	2	2	4	4	2	2	4	4	2	2	4	4	2	2

Figure 3b

# Figure 4



## Cycle Allocation Table

1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	10	10	11	11	12	12	13	13	14	14	15	15	16	16	...
1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	10	10	11	11	12	12	13	13	14	14	15	15	16	16	...
1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	10	10	11	11	12	12	13	13	14	14	15	15	16	16	...
1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	10	10	11	11	12	12	13	13	14	14	15	15	16	16	...
1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	10	10	11	11	12	12	13	13	14	14	15	15	16	16	...

commutator

clock cycles

Figure 5

# Figure 6

## Cycle Allocation Table

commutator	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	1	2	3	4	1	2	5	6	7	8	1	2	3	4	1	2
	15	16	1	2	3	4	1	2	9	10	1	2	3	4	1	2
	14	1	2	15	16	1	2	3	4	5	6	7	8	9	10	11
	13	14	15	16	1	2	3	4	5	6	7	8	9	10	11	12
	12	13	14	15	16	1	2	3	4	5	6	7	8	9	10	11
	11	12	13	14	15	16	1	2	3	4	5	6	7	8	9	10
	10	11	12	13	14	15	16	1	2	3	4	5	6	7	8	9
	9	10	11	12	13	14	15	16	1	2	3	4	5	6	7	8
	8	9	10	11	12	13	14	15	16	1	2	3	4	5	6	7
	7	8	9	10	11	12	13	14	15	16	1	2	3	4	5	6
	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4	5
	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4
	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3
	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2
	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Diagram illustrating the cycle allocation table. The table is a 16x16 grid. A curved arrow labeled "clock cycles" points from the bottom-left corner (1,1) to the top-right corner (16,16), indicating the progression of cycles. The grid is labeled with numbers 1 through 16 in a repeating pattern: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16.